

Design and Power-Performance Optimization of A Low Leakage Serial CAM by using DTCMOS Technique and Transistor Stacks

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Abstract

The Content Addressable Memory (CAM) is a class of memory that allows access by data instead of by physical address. On a read access to a CAM, embedded into a processor cache, each word is compared in a broadcast mode, to see if it matches the requested data; thus requiring only one access. Due to their parallel pattern matching property, CAMs are gaining increasing importance over Random Access Memory (RAM) in recent years, though design complexity and power consumption continue to remain the major drawbacks.

The challenge in the design of a CAM cell is to reduce leakage power in its compare circuitry without sacrificing the speed. This paper describes a novel high-performance low power design of Serial CAM block using Dual-Threshold CMOS (DTCMOS) technique, Transmission Gates (TG), Transistor Stacks and an efficient Match Adaptive Architecture. In this design, for high speed and low power operation, we have used four separate, though not independent techniques. Replacing pass transistors by TG, including transistor stacks in the compare circuitry and assigning appropriate threshold voltages with dual threshold technique have been found to reduce the Power Delay Product (PDP) of the basic serial CAM cell by as much as up to 30%. Switching to a unique Match Adaptive Architecture further improves this Power-Performance of the CAM block significantly as compared to the conventional configuration.

Index Terms – Stack Transistor, Dual Threshold CMOS, TG, PDP, Match Adaptive Architecture

I. Introduction

The 10-transistor (10-Tx) Serial CAM configuration shown in Fig.1 is the basic building block in cache memory organization [1]. Because a CAM is designed to search its entire memory in a single operation, it is much faster than RAM in virtually all kinds of search applications. Unlike a RAM, which has simple storage cells, each individual memory bit in a CAM must have its own associated comparison circuit to detect a match between the stored bit and the input bit.

The extra circuitry in the CAM cell is a source of conspicuous power leakage in the standby mode of operation. Consequently, CAM is only used in specialized applications where searching speed cannot be achieved using a less power hungry method.

In an attempt to achieve a proper balance between speed and standby leakage, this paper presents a power aware design of the serial CAM array intended for ultra low power applications. The novelty of our design lies in the fact that it focuses on the minimization of Power Delay Product (PDP) at the device, circuit and architectural levels of abstraction, all considered together. This three-tier approach in the design of what may be called a **Low Leakage Serial CAM (LLSCAM)** is found to give a reduction in PDP by up to three orders of magnitude.

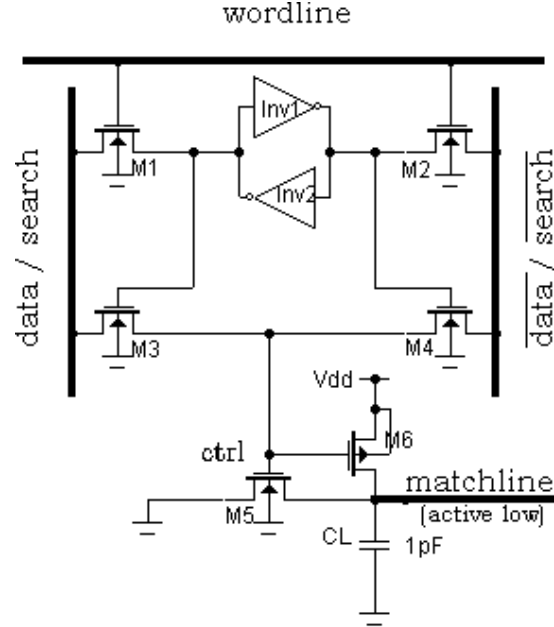


Fig. 1. 10-Tx Basic Single Bit Serial CAM Cell

A. Circuit Operation of the Serial CAM

In a single bit Serial CAM, the word line controls the transistors M1 and M2. When the word line is set *high*, transistors M1 and M2 conduct and data bit enters into the latch. Data bit to be stored in the memory comes from the bus *bit/search* and its compliment from *not(bit)/not(search)*. After the data has been put into the memory, word line need be set *low* to prevent any further modification of the data stored. The transistors M3, M4, M5 and M6 together constitute the compare circuitry of the module. On a match, transistor M5 turns on, connecting the match line to ground. On a miss, match line gets connected to V_{DD} via M6, indicating a data mismatch.

In a multi-bit Serial CAM, a match propagates as a *zero* from the LSB to the MSB of the word. On a hit, a cell turns on its NMOS pass transistor, propagating the result from its less significant neighbor to its next more significant neighbor [1]. If it does not match, it breaks the chain and generates a *one* to pass on without performing any evaluation at the subsequent stages. If the first cell of a set does not match but the second does, a one is propagated through an NMOS transistor.

B. Dual Threshold Principle

In recent years, scaling methodology for low voltage designs is targeted towards constant field scaling by lowering the supply voltage, V_{DD} . The dynamic power dissipation in CMOS circuits is given approximately by

$$P = a f C_L V_{DD}^2 \quad (1)$$

where C_L is the total effective load capacitance at the output node, f , the clock frequency and a , the activity parameter. Lowering V_{DD} reduces the power dissipation quadratically and becomes attractive and almost mandatory for any low power design.

However it causes a problem when the time delay is considered. The time delay T_D is given by

$$T_D = \frac{C_L V_{DD}}{A(V_{DD} - V_T)^\alpha} \quad (2)$$

where A is a constant and α is another constant between 1.4 and 2 depending on the technology [2].

As a result, a low V_{DD} of 1volt leads to drastic performance degradation in the form of slower switching speed. To recoup the performance, the threshold voltage also needs to be reduced. However decreasing V_T makes the transistors difficult to be driven OFF. The sub-threshold leakage current I_{SUB} is given approximately by

$$I_{SUB} = I_{ON} \cdot \exp\left[\frac{C(V_{gs} - V_T)q}{kT}\right] \quad (3)$$

where C is a constant and I_{ON} is the current at $V_{gs}=V_T$.

This causes the standby leakage current to increase significantly in low- V_T transistors. As a result, in the standby or hibernating mode, the low- V_T transistors drain the battery more conspicuously. Power optimization can be achieved if we combine high- V_T and low- V_T transistors in the same chip. The low- V_T transistors can be used for the circuit operation to achieve high speed and high- V_T transistors can be employed for reducing standby leakage power [3]. This method is known as the Dual-Threshold CMOS (DTCMOS) technology.

C. Leakage Control Using Transistor Stacks

Sub-threshold leakage current flowing through a stack of series connected transistors reduces when more than one transistor of the stack is turned off [4]. This effect is known as the "Stacking Effect." The stacking effect is best understood by considering a two-input NAND gate as shown in Fig. 2.

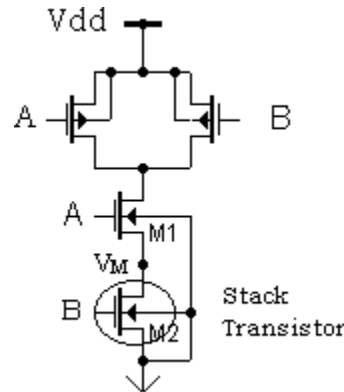


Fig. 2. Stacking Effect in 2-input NAND gate

When both $M1$ and $M2$ are turned off, the voltage at the intermediate node (V_M) is positive due to a small drain current [5]. Positive potential at the intermediate node has the following three effects:

1. Due to positive source potential V_M , gate-to-source voltage of $M1$ (V_{gs_1}) becomes negative and so the sub-threshold current reduces greatly.
2. Due to $V_M > 0$, body-to-source potential (V_{bs_1}) of $M1$ decreases resulting in increasing threshold voltage (more body effect) and thus reducing sub-threshold leakage.
3. For $V_M > 0$, drain-to-source potential (V_{ds_1}) of $M1$ decreases, resulting in increased threshold voltage (less DIBL) and thereby reducing sub-threshold leakage.

The leakage of a two-transistor stack is an order of magnitude less than the leakage in a single transistor [6].

Due to stacking effect, the sub-threshold leakage through a logic gate depends on the applied input vector [4]. In an attempt to reduce the standby leakage power of the serial CAM, an NMOS transistor,

with its gate connected to drain, has been used as stack transistor in the proposed circuit. The stack transistor operates always in saturation and behaves like an active resistor.

II. Simulation & Results

The functional behavior of a CAM can be interpreted in a dual phase operation. During the first phase of the clock cycle, data bit appearing on the data bus enters into the latch and remains stored there. No evaluation (search) takes place in this *Data Write Phase (DWP)*. Match line status evaluation is initiated in the next phase of the clock cycle, when data appearing on the search bus is compared with that stored in the latch in DWP prior to the *Evaluation Phase (EP)*. On a miss, match line undergoes a transition from low-to-high in EP and the *Transition Delay T_D* is defined as the time difference between the instant when the search operation is initiated and the instant when the match line gets charged to 90% of its final value (1 volt) [7]. On a hit, no such delay exists, as no transition takes place.

A. Minimization of PDP using Dual Threshold CMOS Technique:

The SPICE simulation has been performed on 0.2 micron technology with 1 volt supply. The simulations were performed in three different modes:

- (1) Using all low- V_T transistors
- (2) Using all high- V_T transistors
- (3) Using dual- V_T transistors

The circuits have been simulated using Tanner Spice®. For the three modes mentioned above, the net lists are almost similar, only the appropriate device models (high and low- V_T) are to be considered.

The proper choice of threshold voltages for a particular transistor in the circuit is based on a number of logics as described below.

- a. *Placement of high- V_T transistors on the leakage path directly between supply and ground reduces the sub-threshold leakage current and hence static power.*
- b. *Placement of low- V_T transistors on the signal propagation path from the input node to the output improves the performance substantially.*
- c. *A logical intersection of the conditions illustrated in (a) and (b) requires an optimized choice that leads to the minimum PDP.*

It is absolutely transparent from the simulation results shown in Table 1 that the dual- V_T approach offers the minimum PDP for the 10-Tx Serial CAM cell on a data mismatch. The optimum placement of the high- V_T and low- V_T transistors into the circuit has been found to achieve almost 79% reduction in the leakage power as compared to the scheme using all low- V_T transistors and 20% reduction in delay with respect to the high- V_T case. The Serial CAM cell designed using dual- V_T is as fast as with all low- V_T transistors and the least power hungry as well in the standby mode of operation.

Table-1
Simulation results for 10-Tx serial CAM module on data mismatch

Simulation Mode	Leakage Power in 10^{-9} Watt:	Delay in 10^{-9} Sec:	PDP in 10^{-18} Joule:
LOW- V_T	11.40	2.34	26.60
HIGH- V_T	2.40	2.92	7.01
DUAL- V_T	2.40	2.34	5.62

The serial CAM cell shown in Fig. 1 seriously suffers from increased leakage power as indicated in [1]. When the cell matches, **ctrl** is driven high through one of the two NMOS transistors M3 and M4, which lead to a threshold voltage drop. Thus, the PMOS transistor driven by **ctrl** turns off only partially,

allowing substantial leakage through it. The conspicuous drainage of power due to threshold voltage drop can be controlled effectively using transmission gates instead of simple pass transistors.

B. Minimization of Leakage Power on Data Match Using a Transmission Gates (TG):

By replacing the pass transistors M3 and M4 with Transmission Gates (TG), **ctrl** can be pulled high to V_{dd} instead of $(V_{dd}-V_T)$ which in turn reduces the leakage substantially. To drive the transmission gates, no extra clock inverter is needed because of the presence of two cross-coupled inverters in the circuit forming the latch. The effect of replacement of the pass transistors M3 and M4 with a couple of TGs on leakage power reduction is shown in Table 2.

Table-2
Comparison of standby leakage power (in 10^{-9} Watt) on data match

Simulation Mode	10-Tx Serial CAM (Fig. 1)	Serial CAM with TG (Fig. 3)
LOW- V_T	117.00	8.91
HIGH- V_T	7.08	0.95
DUAL- V_T	112.00	3.92

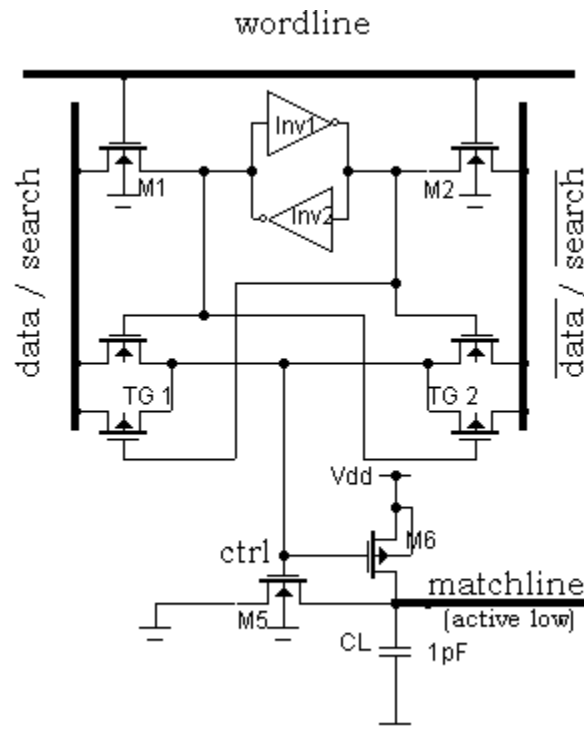


Fig. 3. 12-Tx Transmission Gate Serial CAM

C. Minimization of PDP Using Leakage Control Stack Transistors:

The insertion of stack transistors in a leakage path as described in Section 1.C decreases the sub-threshold leakage current substantially. In our design, we have inserted an NMOS transistor with its drain connected to gate, in series with the transistor M5 (Fig. 4). The leakage current of a stack of off transistors can be modeled and determined by equaling the currents flowing through the series transistors [8]. By increasing the number of off transistors in a stack, the equivalent resistance of the current path between supply and ground is increased and hence, less current flows through the circuit. The sub-threshold leakage current with NMOS stack in series is given by [9].

$$I_{sub} = A e^{(V_G - V_S - V_{th0} - \gamma V_S + \eta V_{DS})} \left(1 - e^{-\frac{qV_{DS}}{kT}}\right) \quad (4)$$

$$\text{where } A = \mu C_{ox} \frac{W}{L_{eff}} \left(\frac{kT}{q}\right)^2 e^{1.8} \quad (5)$$

and V_{DS} is determined using the equation given in [9]

$$V_{DS2} = \frac{nkT}{q(1+2\eta+\gamma)} \ln\left(\frac{A1}{A2} e^{\frac{q\eta V_{dd}}{nkT}} + 1\right) \quad (6)$$

$$V_{DSi} = \frac{nkT}{q(1+2\eta+\gamma)} \ln\left(\frac{A_{i-1}}{A_i} (1 - e^{\frac{q\eta V_{dd}}{nkT}}) + 1\right) \quad (7)$$

$$V_{Si} = \int_{j=i+1}^N V_{DSj} \quad (8)$$

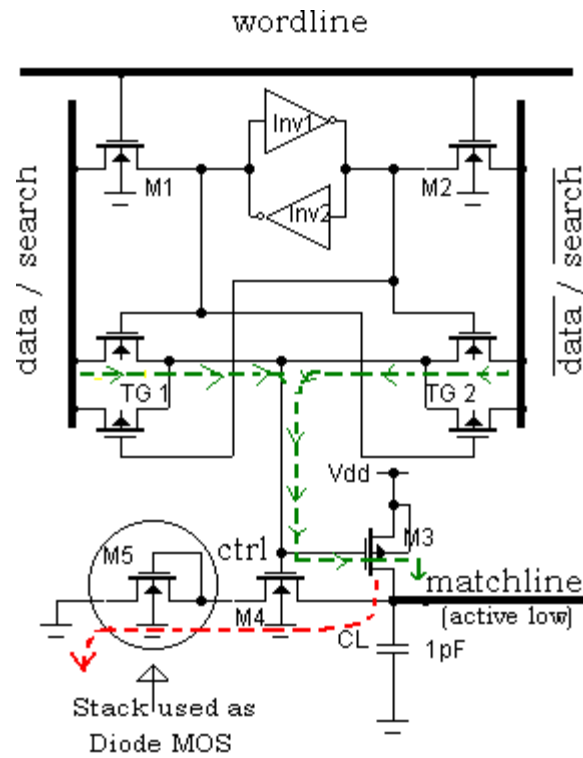


Fig. 4. Low Leakage Serial CAM (LLSCAM) with Stack

In our proposed serial CAM shown in Fig. 4, whenever the data bit appearing on the search bus fails to match the data bit stored in the latch, the control signal propagating along the paths marked by green dotted line ($\rightarrow -$), causes the match line to undergo a $0 \rightarrow 1$ transition. All the transistors placed on this path together determine the search delay in CAM cell. Using dual threshold technique, our primary aim has been to assign low- V_T models to all those transistors placed on the delay determining paths. High- V_T assignment to all other transistors prevents substantial power drainage. Table 3.1 and 3.2 show the simulation results for the Low Leakage Serial CAM (LLSCAM) cell shown in Fig. 4.

Table-3.1
Simulation results for LLSCAM on data mismatch

Simulation Mode	Leakage Power in 10^{-9} Watt:	Delay in 10^{-9} Sec:	PDP in 10^{-18} Joule:
LOW- V_T	9.15	2.30	21.00
HIGH- V_T	2.05	2.90	5.96
DUAL- V_T	1.69	2.26	3.82

TABLE 3.2
Simulation results for LLSCAM on data match

Simulation Mode	Leakage Power in 10^{-9} Watt:
LOW- V_T	8.82
HIGH- V_T	0.95
DUAL- V_T	3.74

It is evident from the simulation results shown in Tables 1 and 3.1 that the PDP for the **Low Leakage Serial CAM (LLSCAM)** configuration (Fig. 4) is almost 30% lower than the 10-Tx Serial CAM configuration (Fig. 1) using dual- V_T design approach. The insertion of a couple of transmission gates in the design of LLSCAM reduces the leakage power by a very large extent on a hit with respect to that of 10-Tx Serial CAM.

D. Delay Minimization Using Leakage Control Stack Transistors:

In our design, the insertion of an NMOS transistor as a leakage control active device not only decreases the sub-threshold leakage current noticeably but as an added advantage, offers also a slight reduction in delay (Table 3.1). This can be explained with the help of an RC equivalent circuit as shown in Fig. 5.

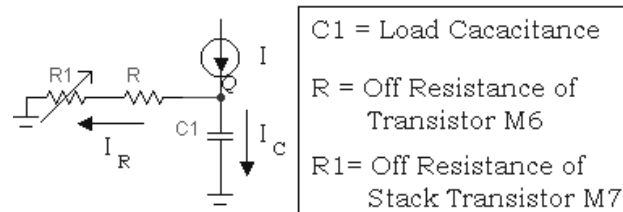


Fig. 5. RC Equivalent of the Compare Circuitry

On a data mismatch, the charging current I_C charges the parasitic capacitance associated with the match line to V_{dd} . Larger the charging current I_C , smaller will be the charging time and hence delay. The total current drawn from V_{dd} through the low- V_T p-transistor M3 gets divided into two components I_C and I_R at node Q. When transistors M4 and M5 (see Fig. 4) are assigned with high threshold voltages, effective series resistance ($R+R1$) (see Fig. 5) of the current path shown by red dotted line (- -) is higher than the case when both the transistors are assigned with low threshold voltages. Hence, the current I_R flowing through the transistors M4 and M5 is less for the first case than the second. In other words, the capacitor charging current I_C is more when M4 and M5 have high- V_T than when their threshold voltages are low. The relative increase of the charging current I_C using dual threshold technique thus accounts for the reduced search delay in case of a mismatch. The reduction in delay for LLSCAM is not that prominent when all high- V_T transistors are used, as then the current I flowing through high- V_T transistor M3 is itself low. Adopting dual threshold technique, a 4% reduction in delay can be achieved in a single bit LLSCAM.

E. Design of an Ultra Low Power CAM Block using Match Adaptive Serial Architecture

Use of a Match Adaptive architecture proposed here offers a significant reduction in PDP for a serial CAM block. The adaptive nature of the CAM architecture reduces both the leakage power and the delay substantially.

The serial part of the Mixed Serial-Parallel CAM (SPCAM) architecture proposed by Efthymiou and Garside in [1] has high standby leakage and increased propagation delay from LSB towards MSB. The serial architecture proposed in this paper not only consumes substantially less power in the standby mode but also reduces the signal propagation delay significantly.

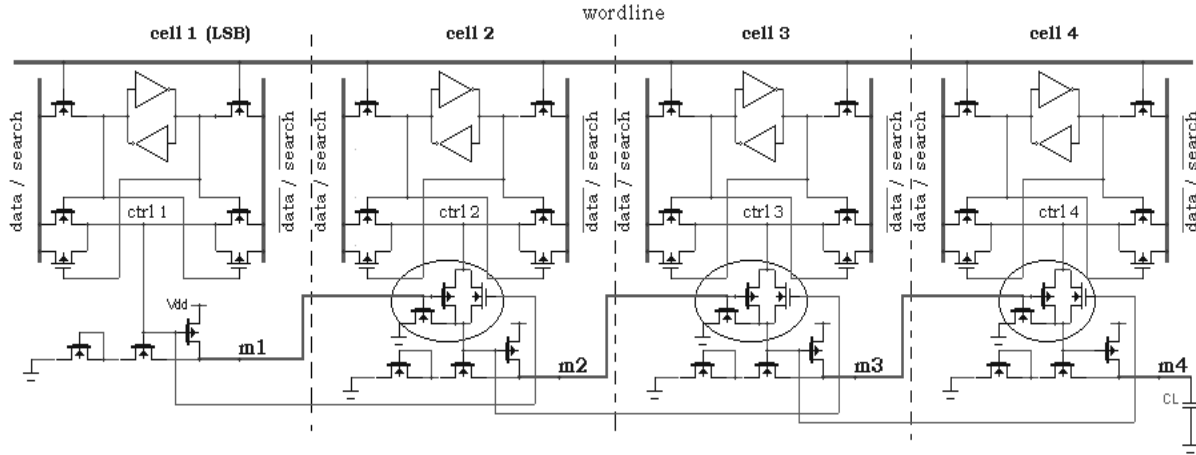


Fig. 6. Four Bit Match Adaptive LLSCAM Architecture

The inherent features that make the proposed CAM architecture shown in Fig. 6 suitable for high speed and ultra low power applications are briefly described below:

- Insertion of control circuitries (marked by the circles) in the individual cells except the left most “cell 1” incorporates *Match Adaptability* to the serial CAM array. The match adaptive propagation structure ensures that a hit or a miss decision at the n^{th} bit position of the array depends upon the search results (a hit or a miss) of the $(n-1)^{\text{th}}$ bit positions prior to that. If a mismatch occurs at “cell 1”, node m1 is pulled up to logic high which eventually connects the node m2 to Vdd. This continues until m4 gets charged to Vdd indicating a tag mismatch. It is to be noted that having a mismatch at “cell 1”, no further evaluation takes place in the subsequent bit positions. On a mismatch at any particular bit position of the array, the elimination of bit comparisons at all the subsequent stages offers a 50% reduction in propagation delay as compared to the SPCAM architecture proposed in [1].

Table-4
Different HIT / MISS conditions in a 4-bit serial CAM array

State	Cell 1	Cell 2	Cell 3	Cell 4
1	M	M	M	M
2	M	M	M	H
3	M	M	H	M
---	---	---	---	---
15	H	H	H	M
16	H	H	H	H

$M \rightarrow \text{Miss}, H \rightarrow \text{Hit}$

In case of a serial search scheme, assuming a 50% probability of a match at any particular bit position for each word, the probability of a word not matching after N bits can be written as [1]:

$$P_{\text{miss}} = \left(\frac{1}{2}\right) + \left(\frac{1}{2}\right)^2 + \dots + \left(\frac{1}{2}\right)^N = 1 - \left(\frac{1}{2}\right)^N \quad (9)$$

For $N = 4$, we notice that in more than 93% of search cases the input data fails to match with that stored in the CAM. Since over 90% of the mismatches can be covered only within the four least significant bits (starting from cell 1 to cell 4), it is sufficient enough to consider a 4 bit serial CAM array for the purpose of simulation.

In a 4 bit serial CAM array, a total of 16 ($=2^4$) different hit/miss conditions have been considered for each of the three different simulation modes (Viz. low- V_T , high- V_T and dual- V_T) as illustrated in Table 4. The average PDP for each mode has been calculated according to the formula written below:

$$\overline{\text{PDP}} = \frac{1}{16} \sum_{i=1}^{16} P_i D_i \quad (10)$$

where

P_i = Leakage Power for the i^{th} simulation state

D_i = Propagation Delay corresponding to the i^{th} state.

The simulation results for both the SPCAM and Match Adaptive architecture are shown in Table 5.

Table-5

PDP comparison between SPCAM & match adaptive SERIAL CAM architecture

	Simulation Mode	Leakage Power in 10^{-9} Watt:	Delay in 10^{-9} Sec:	PDP in 10^{-18} Joule:
SPCAM Architecture	LOW- V_T	1050.00	5.76	6020.00
	HIGH- V_T	388.00	6.92	2680.00
	DUAL- V_T	1020.00	5.96	6070.00
Match Adaptive Architecture	LOW- V_T	34.80	2.64	91.60
	HIGH- V_T	10.00	3.41	35.60
	DUAL- V_T	8.46	2.66	21.10

It is evident from Table 5 that the proposed Match Adaptive Serial Architecture is eminently suitable for ultra low power as well as high speed applications as compared to SPCAM proposed in [1].

- b. Another advantage of the proposed serial CAM architecture lies in the fact that the propagation delay decreases linearly with the number of mismatches from LSB to MSB (Table 6). The reduction in propagation delay with the number of misses in the consecutive bit locations seems to be very useful in the worst case scenario, when all the input bits fail to match the bits stored in a row. In other words, the proposed architecture is somewhat capable of sensing partial matches.

Table-6

Reduction of propagation delay with the number of mismatches from LSB towards MSB

Cell 1	Cell 2	Cell 3	Cell 4	Propagation Delay in ns		
				High- V_T	Low- V_T	Dual- V_T
M	H	H	H	4.05	3.15	3.18
M	M	H	H	3.96	3.06	3.10
M	M	M	H	3.83	2.92	2.96
M	M	M	M	3.64	2.74	2.77

$M \rightarrow$ Miss, $H \rightarrow$ Hit

The reason behind such a smart behavior of the architecture shown in Fig. 6 can be explained with the help of a circuit model as shown in Fig. 7.

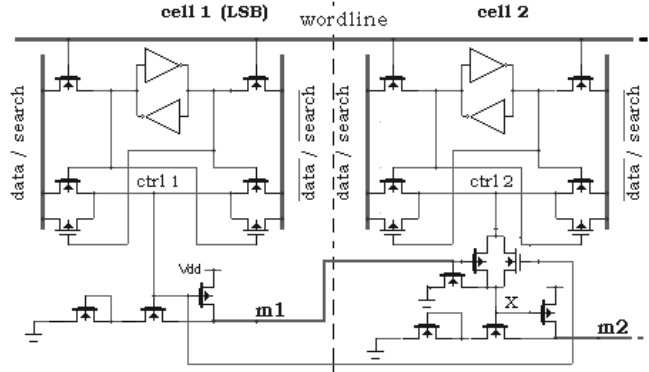


Fig. 7 Circuit Model explaining the Smart Architectural Behavior

During the Data Write Phase (DWP), the intermediate match line m1 remains pre discharged as the node “ctrl 1” is pulled high by either data or not(data) bus lines. This keeps the transmission gate between the nodes “ctrl 2” and “x” conducting. The process of writing data to cell 2 also causes the node “ctrl 2” to remain at logic ‘1’ which in turn charges the node “x” to logic high. Now we shall consider two cases.

Case: 1 (Miss at “Cell 1” but Hit at “Cell 2”)

At the beginning of the Evaluation Phase (EP), “ctrl 1” undergoes a 1→0 transition but “ctrl 2” remains at logic ‘1’. As the logic transition involves a finite charging time delay, the transmission gate between node “ctrl 2” and “x” conducts for a little while before it is switched off by m1. As both “ctrl 2” and “x” stay at logic ‘1’, this brief span of conduction through transmission gate doesn’t contribute much to the reduction of propagation delay. The correct logic output at node “m2” is obtained only after the entire charge stored at node “x” gets discharged via the NMOS pass transistor. The propagation delay in this case can be formulated as:

$$T_{p1} = T_0 + \tau_1 \quad (11)$$

where

T_0 = Offset Delay due to signal propagation from “ctrl 1” to “m1” at the beginning of EP, and

τ_1 = Discharging time for the entire charge stored at node “x” during DWP.

Case: 2 (Miss at both “Cell 1” and “Cell 2”)

At the beginning of EP, both “ctrl 1” and “ctrl 2” undergo a 1→0 transition at the same time. After the transition, node “ctrl 2” comes to logic ‘0’. There after, within the brief span of conduction, a fraction of charge stored at “x” during DWP gets discharged through the transmission gate. The correct logic output at node “m2” is obtained after the remaining charge stored at “x” drained via the NMOS pass transistor. Therefore the propagation delay can be expressed as:

$$T_{p2} = T_0 + \tau_2 \quad (12)$$

where

T_0 = Offset Delay due to signal propagation from “ctrl 1” to “m1” at the beginning of EP, and

τ_2 = Discharging time for a *fraction* of the entire charge stored at node “x” during DWP.

As $\tau_2 < \tau_1$, $T_{p2} < T_{p1}$

III. Conclusions

The design of a high performance Low Leakage Serial CAM (LLSCAM) has been proposed in this paper. Our attempt throughout this piece of work has been to reduce the power consumption as well as the propagation delay in the four LSBs of the cache tag which are sufficient to cover more than 93% of tag misses. Proper modifications at the device, circuit and architectural levels of design hierarchy reduce the

Power Delay Product (PDP) for a four bit serial CAM array by almost up to three orders of magnitude in comparison with that of SPCAM array proposed by Efthymiou and Garside. The power efficient design of the serial CAM sub block proposed by us potentially adds value to the original SPCAM architecture making it suitable for use in ultra low power caches embedded into modern microprocessors.

In addition, the Match Adaptive Serial architecture proposed in our design efficiently propagates the status signal from LSB towards MSB without performing redundant checking at all bit locations of the array reducing the delay overhead noticeably. The ability of this adaptive architecture to sense partial data match in between and adjust the data path delay accordingly offers as much as up to 13% improvement in the search speed under worst case scenario.

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